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(54) Title: METHOD AND APPARATUS FOR DIRECT SYNCHRONOUS RECTIFICATION IN A PULSE-WIDTH MODULATED MOTOR CONTROLLER

(57) Abstract: A direct synchronous rectification system characterized by a reduction in the number of operational components as compared with conventional systems is disclosed. In one embodiment, the rectifier comprises a power switching module comprising six switches and six associated diodes. Each phase of the incoming three-phase signal is coupled by a first diode to a positive DC bus bar and by a second diode to a negative DC bus bar. The six switches are adapted to selectively establish a short-circuit path for current from the DC bus to the source of AC power. Control circuitry is provided to close each switch during at least a portion of each interval in which current is flowing through diode associated with that switch. A low-capacitance DC bus capacitor is disposed between the positive and negative DC bus bars.

METHOD AND APPARATUS FOR DIRECT SYNCHRONOUS RECTIFICATION IN A PULSE-WIDTH MODULATED MOTOR CONTROLLER

FIELD OF THE INVENTION

This invention relates generally to the field of electric motors, and more particularly to a method and apparatus for direct synchronous rectification of a three-phase supply voltage without a pulse-width modulated carrier to generate a direct current output voltage with bidirectional current flow capability.

BACKGROUND OF THE INVENTION

Variable-speed alternating-current ("AC") induction motors, and the control systems for operating such motors, are well-known in the art. In typical systems, the rotational speed of the motor is controlled through adjustment of the frequency of the AC power supplied to the motor. Because AC power is supplied from electrical utilities at a substantially constant frequency (typically 60 Hz), it is not possible to apply electrical power directly to a variable-speed motor. As a result, variable-speed motor controllers must include circuitry for deriving a variable-frequency AC signal from the fixed-frequency signal provided from the utility.

The most common method for generating the variable-frequency AC power signal for driving an AC induction motor involves two main steps: First, the fixed-frequency AC signal supplied by the utility is converted into an intermediate DC signal, a process called rectification of the AC signal. Next, the variable-frequency AC signal is derived from the intermediate DC voltage. This latter process is commonly accomplished using pulse-width modulation ("PWM") techniques involving a plurality of diodes and electrical switches such as insulated-gate bipolar transistors ("IGBTs"). Numerous methods and variants for rectification of AC signals and derivation of AC signals from DC signals are well-known to those of ordinary skill in the art.

A typical synchronous rectifier for a motor control system comprises a line reactor, a power switching module, a large electrolytic bus capacitor, and control circuitry, often microprocessor-based, for controlling the power module using PWM. The control circuitry evaluates incoming three-phase AC voltages and the outgoing DC voltage, and controls the PWM signals applied to the power module so as to regulate the DC output voltage to desired levels. The technology associated with such control systems is highly developed and has proven effective in a great many applications.

One consideration relating to the production of variable-frequency AC signals arises out of the natural ability of a standard AC induction motor to act as a generator, if it has excitation (power) present and its shaft is turning faster than the applied AC drive frequency. This condition, sometimes referred to as regeneration, can occur if there is a large mass (inertia) on the shaft and the drive is decelerating. This can happen during a normal stop or when the motor is changing speeds from fast to slow in a short period of time.

When a motor is acting as a generator, the regenerated power is directed back from the drive circuitry controlling the motor. The excess energy flows from the motor to the drive. This can cause the intermediate DC voltage to rise, and can eventually cause an overvoltage condition on the DC bus. In order to avoid this, the excess (regenerated) energy must be removed from the drive.

There are at least two methods for dissipating regenerated energy in a motor controller. One method is known as resistive or dynamic braking. When the DC bus voltage in the drive rises, a resistive load is connected across the drive's DC bus by means of a semiconductor switch. The excess energy is turned into heat. Another method is called regenerative braking. With regenerative braking, the energy coming from the motor is transferred back to the power utility (variously referred to as "the power grid" or simply "the grid") and absorbed. The latter method is deemed preferable in some applications, since no heat is produced, and no resistors, which tend to be bulky and inefficient, are needed. Further, regenerative braking has the added beneficial side-effect of reducing consumption of power from the grid, which in turn leads to lower utility costs for the power consumer. Numerous examples of motor drives having either resistive braking or regenerative braking are well-known and commercially-available.

Among the well-known characteristics of typical PWM motor drive systems is that the control circuitry, especially that associated with regenerative braking, is typically rather complex, requiring a significant investment in both software and hardware to develop and manufacture. The complexity of conventional PWM motor control systems renders such systems less reliable, being more susceptible to malfunction and/or breakdown, and increases the associated costs. In addition, the bus capacitor in many conventional motor control systems exhibits a limited lifetime as it dries out due to the heat of the core during use.

Accordingly, it would be desirable to provide a simplified motor control arrangement for conventional applications.

SUMMARY OF THE INVENTION

In view of the foregoing considerations, the present invention is directed in one respect to a method and apparatus for direct synchronous rectification without a control system and without a pulse width modulated carrier. In one embodiment, the invention involves the use of a low-capacitance bus in place of a conventional synchronous rectifier, resulting in reduced cost, improved reliability, improved lifetime, improved time-to-market, and simplified circuitry.

In accordance with one aspect of the invention, the disclosed system comprises a power switching module including six diodes and six associated switches, as well as a switching control circuit for generating control signals to control the opening and closing of the switches. Each of the three phases of the incoming AC signal is coupled by a first diode to a positive DC bus bar and by a second diode to a negative DC bus bar. In one embodiment, each switch is controlled to provide a short-circuit path across the diode with which it is associated for at least a portion of the time that current is flowing through the diode. The short-circuit provides a path for regenerated current to flow from the positive and negative DC buses to the AC power source.

Advantageously, the synchronous rectifier in accordance with the present invention improves system reliability as compared with convention synchronous rectifiers as a result of the simplicity of design and reduction in the number of functional components. Further, the simplicity resulting from the principles of the present invention tends to reduce the cost of the overall system.

In accordance with another aspect of the invention, a lower-capacitance DC bus capacitor is substituted for the conventional high-capacitance bus capacitor. Reducing the DC bus capacitance reduces bus capacitor temperature rise and reduces incoming power line currents.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other features and aspects of the present invention will be best understood with reference to the following detailed description of a specific embodiment of the invention, when read in conjunction with the accompanying drawings, wherein:

Figure 1 is a simplified block diagram of a conventional synchronous rectifier system;

Figure 2 is a simplified block diagram of a synchronous rectifier system in accordance with one embodiment of the invention;

Figure 3 is a schematic diagram of the power switching module in the synchronous rectifier system of Figure 2; and

Figure 4 is a signal timing diagram showing the states of control signals applied to the power switching module from Figure 3.

DETAILED DESCRIPTION OF A SPECIFIC EMBODIMENT OF THE INVENTION

In the disclosure that follows, in the interest of clarity, not all features of actual implementations are described. It will of course be appreciated that in the development of any such actual implementation, as in any such project, numerous engineering and design decisions must be made to achieve the developers' specific goals and subgoals (e.g., compliance with system- and business-related constraints), which will vary from one implementation to another. Moreover, attention will necessarily be paid to proper engineering and design practices for the environment in question. It will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the field of motor control/drive and synchronous rectification systems.

Referring to Figure 1, there is shown a block diagram of a conventional prior art synchronous rectifier system 10. As discussed above, system 10 is notable for its relative complexity. System 10 comprises a three-coil line reactor 12 coupled to receive a three-phase alternating current (AC) power input on three incoming lines designated PhA, PhB, and PhC in Figure 1. At least two of the three phases out of reactor 12 are applied to current sensing circuits 14 and 16. All three phases are then applied to a conventional PWM diode bridge and insulated-gate bipolar transistor (IGBT) switching circuit 18. The DC output of diode/IGBT circuit 18 is applied to a DC bus 20. A (typically) large electrolytic bus capacitor 21 is coupled between the respective positive (+BUS) and negative (-BUS) DC bus rails. DC bus 20, in turn, is applied to the inputs of a PWM controller (not shown) for generation of a variable-frequency AC signal in accordance with conventional methods. An inductive soft start control circuit 13 may also be included to control the charging of the DC bus 20, in accordance with known practices.

To achieve the necessary output voltage regulation, a type of feedback arrangement may be employed wherein the DC bus 20 is applied, as shown in Figure 1, to a buffer 22, the output of which being applied to one input of a differential amplifier 24. Differential amplifier 24 compares the DC voltage on bus 20 to a reference voltage V_{ref} and generates an output voltage that is applied

to the input of a gain control circuit 26. Gain control circuit 26, in turn, generates a reference signal that is applied to one input of two multiplier circuits 28 and 30. A second input of multiplier 28 receives one phase of the three-phase AC input signal; likewise, a second input of multiplier 30 receives another phase of the three-phase AC input signal.

A differential amplifier 32 receives the output of multiplier 28 at one input and an output signal from current sensing circuit 14 at another input to produce a first differential output that is applied to the input of a first gain control circuit 36. A differential amplifier 38 receives the output of multiplier 30 at one input and an output signal from current sensing circuit 16 at another input to produce a second differential output that is applied to the input of a second gain control circuit 40. Gain control circuits 36 and 40 produce analog signals to control the operation of pulse width modulating driver circuits 42 and 44, respectively. The analog signals from gain control circuits 36 and 40 are applied to the inputs of an inverting average circuit 46 to derive a PWM signal to control the operation of a third pulse width modulating driver circuit 48.

Those of ordinary skill in the art will be familiar with the manner in which the feedback loop depicted in Figure 1 enables a desired DC voltage on DC bus 20 to be maintained on a dynamic basis. As can be appreciated with reference to Figure 1, however, such an arrangement adds substantial complexity to the overall synchronous rectifier circuit, increasing the circuit's cost and susceptibility to failure. Additionally, DC bus capacitor typically exhibits a limited lifetime as it dries out due to heating of the core during typical use.

Turning to Figure 2, there is shown a simplified block/schematic diagram of a direct synchronous rectifier system 50 in accordance with one embodiment of the invention. As shown in Figure 2, direct synchronous rectifier 50 comprises a three-coil line reactor 52, an IGBT/diode power switching module 54, and an IGBT gate control module 56. Reactor 52 and switching module 54 are substantially the same as reactor 12 and switching module 18 in the prior art embodiment depicted in Figure 1.

In the embodiment of Figure 2, the large bus capacitor is replaced with a substantially smaller capacitor 58, which may be, for example, a polypropylene capacitor with a capacitance of only approximately three percent of typical bus capacitance. As shown in Figure 2, capacitor 58 is disposed between positive (+BUS) and negative (-BUS) DC bus rails 60.

Referring now also to Figure 3, there is shown a schematic diagram of power switching module 54 in accordance with the presently disclosed embodiment of the invention. As can be seen

in Figure 3, switching module 54 comprises a plurality (six) of diodes 62, 64, 66, 68, 70, and 72, and a corresponding plurality of switches 74, 76, 78, 80, 82 and 84. In accordance with conventional implementations, switches 74-84 are preferably IGBT devices characterized by their fast switching times and high voltage ratings. For clarity, lines coupling the control signals provided from IGBT gate control circuit 56 to the gates of the respective switches 74-84 are not shown in Figure 3.

Figure 4 is a timing diagram showing the gate control signals generated by IGBT gate control circuit 56 to control the opening and closing of switches 74-84 in switching module 54. Also shown in Figure 4 are the three phases $\phi 1$, $\phi 2$, and $\phi 3$ of AC voltage applied to switching circuit 54 by reactor 52. In Figure 4, reference numeral GC74 is used to identify the gate control signal applied to IGBT 74 in Figure 3, reference numeral GC76 is used to identify the gate control signal applied to IGBT 76 in Figure 3, and so on. It is to be understood that assertion of any particular gate control signal GC74-GC84 corresponds to the closing of the corresponding switch in Figure 3.

From Figures 3 and 4, it is apparent that gate control circuit 56 turns each respective switch 74-84 on only during the time that current is flowing through the diode with which it is paired; the closing of each switch results in the establishment of a short-circuit across the corresponding diode. For example, from Figures 3 and 4, it is apparent that switch 76 is closed only during the interval designated T1 in Figure 4 when a positive voltage on $\phi 1$ causes current flow through diode 76. Closing switch 76 establishes a short-circuit current path between positive DC bus bar +BUS and the $\phi 1$ line. Likewise, switch 74 is closed only when a negative voltage on $\phi 1$ causes current flow through diode 62, creating a short-circuit current path between negative DC bus bar –BUS and the $\phi 1$ line, and so on. Establishing these short-circuit current paths across the respective diodes enables regenerative power to flow back to the power line without the necessity of providing a control circuit.

In one embodiment, during successive power line switching events as described with reference to Figure 4, a switch is preferably turned on just before (e.g., 800 nanoseconds or so before) the neighboring switch is turned off. This results in unconditional, continuous zero voltage switching.

With continued reference to Figure 3, in the presently disclosed embodiment, the inductance of three-coil reactor 52 cooperates with bus capacitor 58 to function as a soft-start mechanism to allow bus capacitor 58 to charge at a limited rate with limited current. That is, reactor 52 resonates with the low-valued bus capacitor 58, allowing the bus voltage to rise to a final value at a controlled

current. Such resonant ring-up concept is believed to be more rugged and much faster than conventional solid-state soft-start switches.

The direct synchronous rectification system 50 in accordance with the presently disclosed embodiment of the invention is believed to offer significant advantages over previous designs. The simplicity of the design in accordance with the presently disclosed embodiment decreases the cost of the rectifier while at the same time increasing overall reliability and minimizing the likelihood of component failure. The reduced DC bus capacitance as compare with conventional designs likewise offers potential advantages. For example, if one phase of the incoming AC current is disabled for some reason when the bus is loaded, the lower bus capacitance causes the bus voltage to decrease more rapidly than with conventional designs. This enables phase loss to be detected quickly without employing elaborate phase loss detection circuitry.

From the foregoing detailed description of specific embodiments of the invention, it should be apparent that a method and apparatus for direct synchronous rectification of a three-phase supply voltage to produce a regulated DC output voltage has been disclosed. Although specific embodiments of the invention have been disclosed herein in some detail, this has been done solely for the purposes of illustrating various aspects and features of the invention, and is not intended to be limiting with respect to the scope of the invention. It is contemplated that various substitutions, alterations, and/or modifications, including but not limited to those design alternatives which might have been specifically noted in this disclosure, may be made to the disclosed embodiment without departing from the spirit and scope of the invention as defined in the appended claims.

CLAIMS:

1. A method of synchronous rectification of a three-phase AC signal from an AC signal source, comprising:

(a) coupling a first phase of said AC signal to a positive DC bus bar via a first diode and to a negative DC bus bar via a second diode;

(b) coupling a second phase of said AC signal to said positive DC bus bar via a third diode and to said negative DC bus bar via a fourth diode;

(c) coupling a third phase of said AC signal to said positive DC bus bar via a fifth diode and to said negative DC bus bar via a sixth diode;

(d) for each of said first, second, third, fourth, fifth and sixth diodes, providing a short-circuit across said diode during at least a portion of each interval in which current is flowing across said respective diodes, thereby establishing a path for regenerative current on said positive and negative DC bus bars to flow to said AC signal source.

2. A method in accordance with claim 1, further comprising:

(e) disposing a bus capacitor between said positive and negative DC bus bars.

3. A method in accordance with claim 2, wherein said bus capacitor is a polypropylene capacitor.

4. A synchronous rectifier system, comprising:

a three-coil reactor adapted to interface with a source of a three-phase AC signal to derive first, second, and third phase signals $\phi 1$, $\phi 2$, and $\phi 3$, respectively;

a power switching module coupled to receive said phase signals $\phi 1$, $\phi 2$, and $\phi 3$ from said three-coil reactor;

a gate control module coupled to said source of a three-phase AC signal and to said power switching module;

wherein said power switching module comprises:

a first diode coupled between said first phase signal $\phi 1$ and a positive DC bus bar;

a second diode coupled between said first phase signal $\phi 1$ and a negative DC bus bar;

a third diode coupled between said second phase signal $\phi 2$ and said positive DC bus bar;

a fourth diode coupled between said second phase signal $\phi 2$ and said negative DC bus bar;

a fifth diode coupled between said third phase signal $\phi 3$ and said positive DC bus bar;

a sixth diode coupled between said third phase signal $\phi 3$ and said negative bus bar;

a first switch for selectively providing a short-circuit current path across said first diode;

a second switch for selectively providing a short-circuit current path across said second diode;

a third switch for selectively providing a short-circuit current path across said third diode;

a fourth switch for selectively providing a short-circuit current path across said fourth diode;

a fifth switch for selectively providing a short-circuit current path across said fifth diode;

a sixth switch for selectively providing a short-circuit current path across said sixth diode;

wherein said gate control module is responsive to said three-phase AC signal to generate control signals applied to said first, second, third, fourth, fifth, and sixth switches such that for each of said first, second, third, fourth, fifth, and sixth switches, respectively, a short-circuit current path is established thereacross for at least a portion of each interval when current is flowing through said respective diode.

5. A synchronous rectifier system in accordance with claim 4, further comprising a DC bus capacitor coupled between said positive and negative DC bus bars.

6. A synchronous rectifier system in accordance with claim 5, wherein said DC bus capacitor is a polypropylene capacitor.

7. A synchronous rectifier in accordance with claim 4, wherein each of said first, second, third, fourth, fifth and sixth switches comprises an insulated gate bipolar transistor.

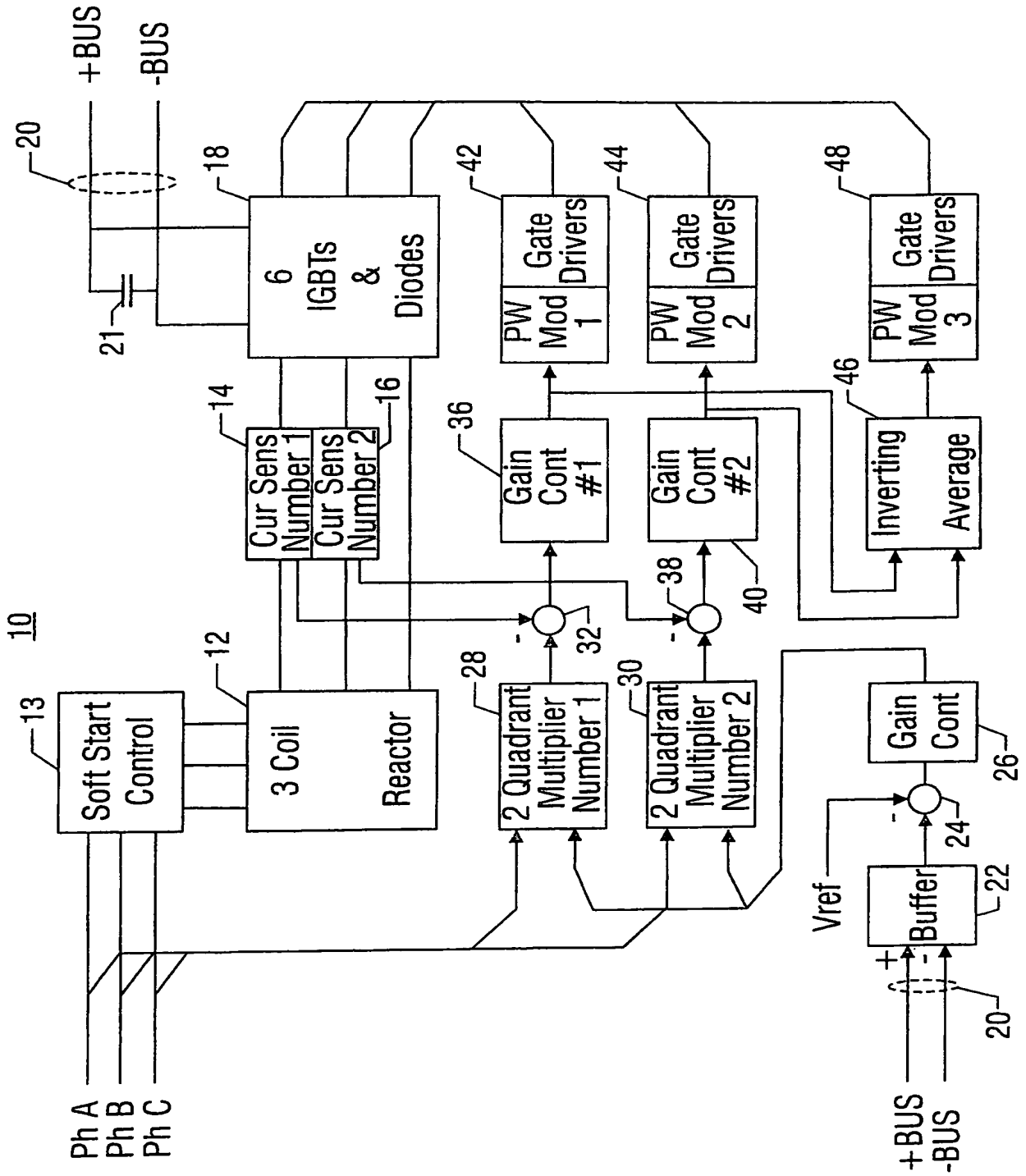
+BUS
-BUS
20
21
18
6 IGBTs & Diodes
42
PW Mod 1
Gate Drivers
44
PW Mod 2
Gate Drivers
48
PW Mod 3
Gate Drivers
14
Cur Sens Number 1
Cur Sens Number 2
16
36
Gain Cont #1
Gain Cont #2
38
40
46
Inverting Average
10
12
13
Soft Start Control
3 Coil Reactor
28
2 Quadrant Multiplier Number 1
30
2 Quadrant Multiplier Number 2
32
Gain Cont
26
24
Vref
Buffer
22
Ph A
Ph B
Ph C
+BUS
-BUS

FIG. 1

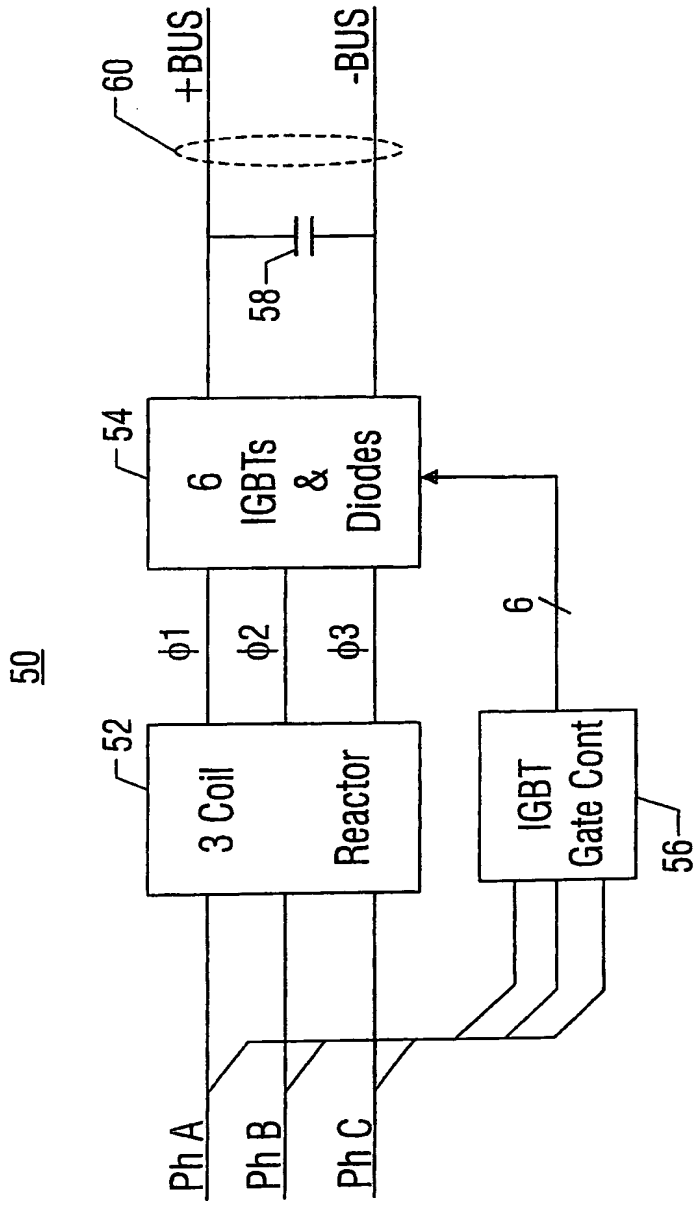
50
60
+BUS
-BUS
58
54
6
IGBTs
&
Diodes
φ1
φ2
φ3
6
52
3 Coil
Reactor
IGBT
Gate Cont
56
Ph A
Ph B
Ph C

FIG. 2

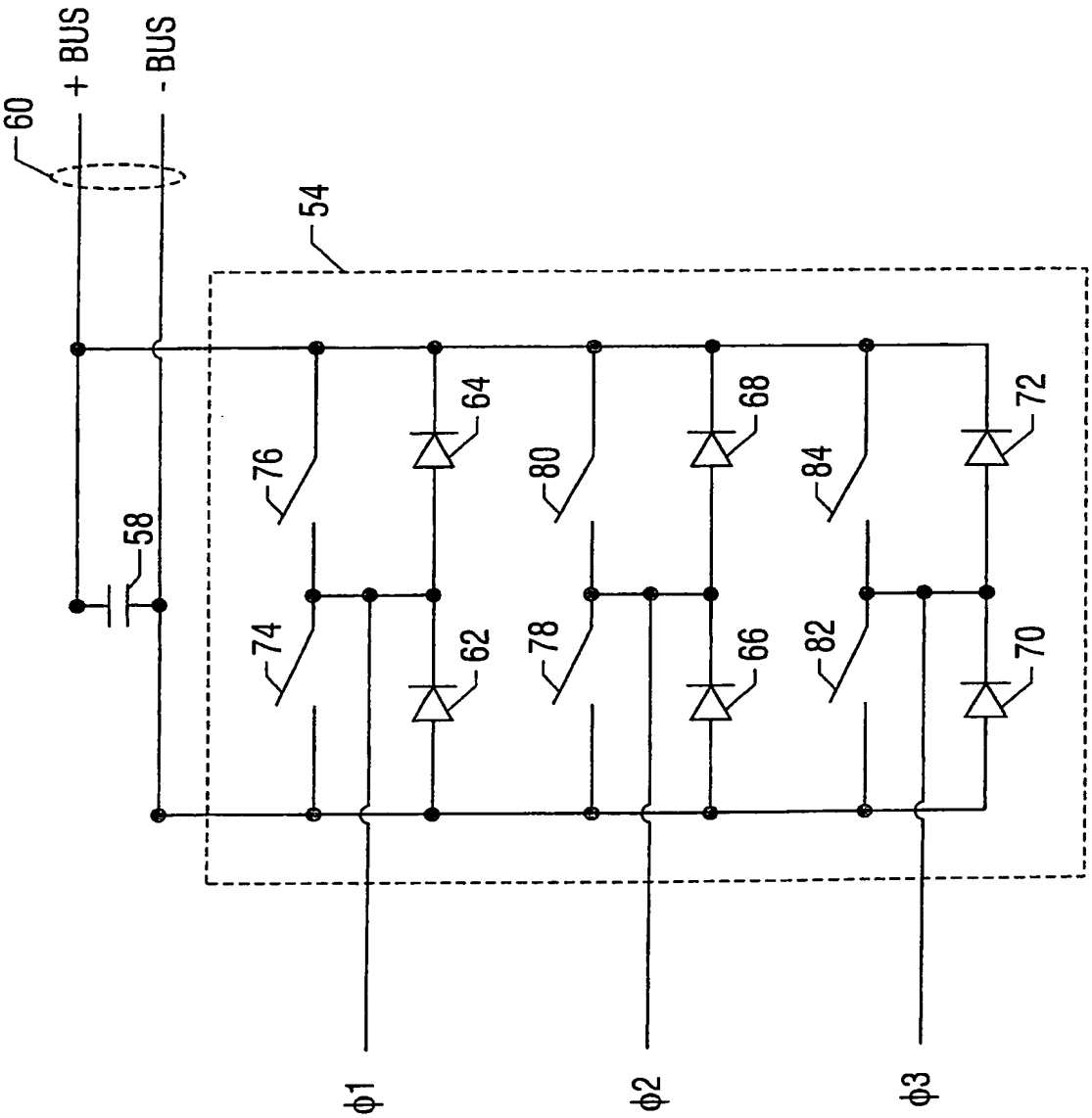

FIG. 3

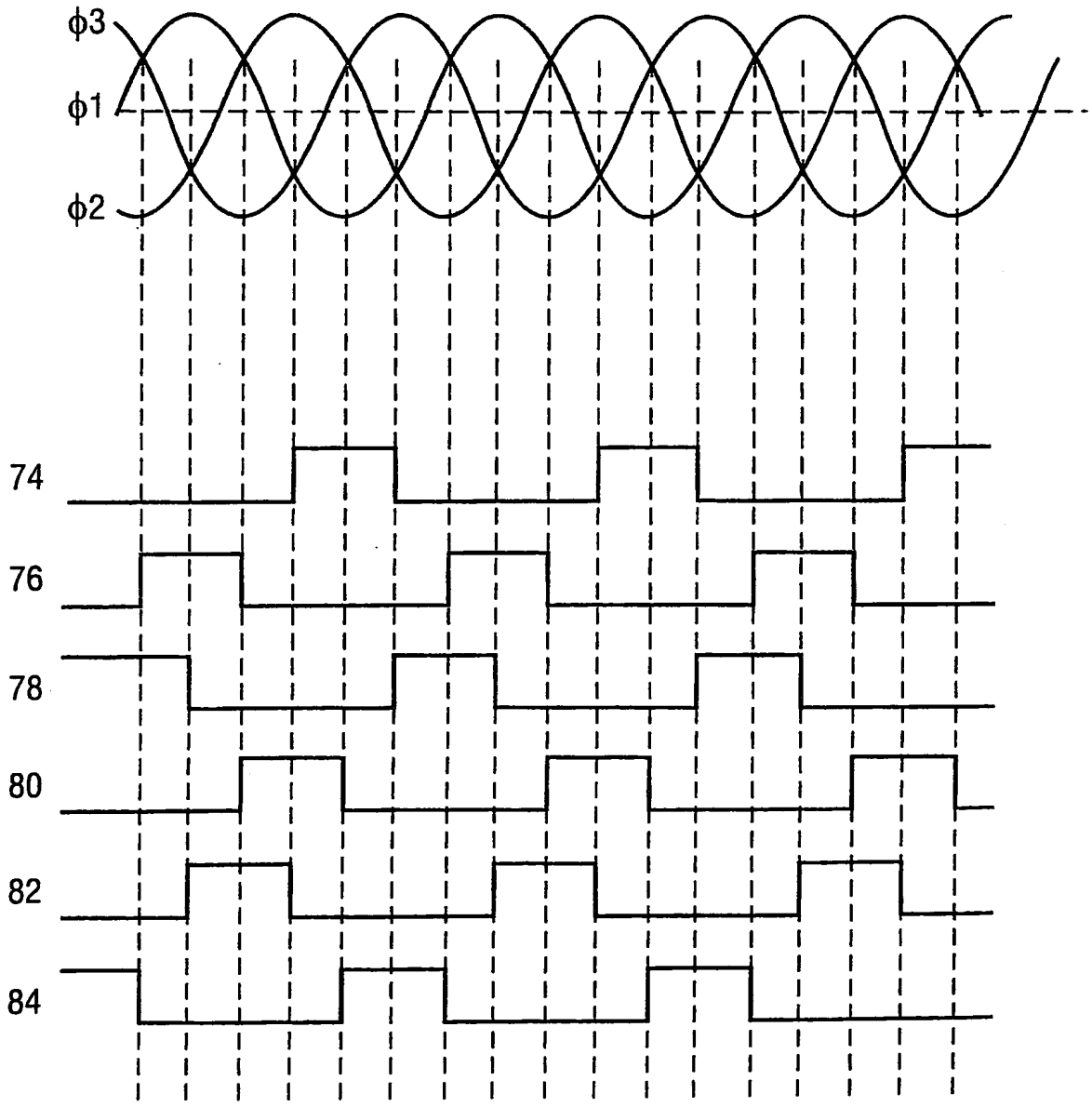

FIG. 4